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IN THE SPECIFICATION

[0015] In accordance with this invention, a method is provided for fabricating an FET device by the following steps. Form a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material. Form a channel structure over the horizontal surface of the substrate connecting between the drain region and the source region, with the channel structure comprising a ~~horizontal~~ horizontally extending, semiconductor, planar channel fin formed above a vertical fin with the planar ~~fin~~ and ~~the~~ vertical fins having a T-shaped cross-section, [[, the]] The vertical fin ~~having~~ has a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin. Form a gate dielectric layer over exposed surfaces of the channel structure. Then form a gate electrode straddling the channel gate dielectric and the channel structure.

[0022] In accordance with another aspect of this invention, an FET device includes a semiconductor structure comprising a source region, a drain region over a horizontal surface of a substrate comprising an insulating material. A channel structure over the horizontal surface of the substrate connects between the drain region and the source region, with the channel structure comprising a ~~horizontal~~ horizontally extending, semiconductor, planar channel fin formed above a vertical fin with the planar ~~fin~~ and ~~the~~ vertical fins having a T-shaped cross-section, ~~with the~~ The vertical fin ~~having~~ has a proximal edge and a distal edge, with the proximal edge in contact with the horizontal surface of the substrate and with the planar fin in contact with the distal edge of the vertical fin. A gate dielectric layer overlies exposed surfaces of the channel structure. A gate electrode straddles the channel gate dielectric and the channel structure.

[0030] FIG. 1C is a modification of the device of FIG. 1A in which the height of the single fin has been reduced to 2/3H, thereby yielding an overall edge contact between the fin and the gate electrode with a width of (4/3)H.